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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 07/14/2004

23

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/700,874	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18-31,36-39,41 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7 and 31* is/are allowed.

6)☒ Claim(s) *1-5,8-16,18-30,36-39,41 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on April 28, 2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 8-16, 18-30 and 38-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Ninomiya et al. (USPN: 5,819,054).

Regarding claims 1 and 8, Ninomiya discloses a disk array controller (Figure 1) comprising a channel interface package in which at least a channel interface unit with a host computer and access path interface are packaged (Figure 1, Reference 1; the channel interface unit is the internal logic coupled to the host interface and the access path interface is the internal logic coupled to bus Reference 4 in Figure 1); a disk interface package in which at least a disk interface with a disk drive and an access path interface unit are packaged (Figure 1, Reference 2; disk interface is the internal logic coupled to Reference 5 in Figure 1 and the access path interface is the internal logic coupled to Reference 4); and a memory package in which a memory unit for storing control data for the disk drive and an access path interface unit are packaged (Figure 1, Reference 3; the access path interface unit is the internal logic coupled to Reference 4 in Figure 1); wherein connections are made between the access path interface unit in

the channel interface package and the access path interface unit in the memory package by first cables (Figure 20, Reference 207-1) and between the access path interface unit in the disk interface package and the access path interface unit in the memory package by second cables different from the first cables [Figure 20, Reference 208-1) (the connections are made between the access path interface unit in the channel interface package and the access path interface unit in the memory package and between the access path interface unit in the disk interface package and the access path interface unit in the memory package by cables (Reference 4 in Figure 1; a bus is a collection of wires used to connect internal components and thus the bus making the above connections is the cable).

Regarding claims 2 and 9, Ninomiya discloses the disk array controller comprising plural memory packages, wherein connections are made between the access path interface unit in the channel interface package via the first cables an the access path interface unit in each of the plural memory packages by second cables different from the first cables (Figure 1, Reference 3).

Regarding claims 3 and 10, Ninomiya discloses the plural memory packages interconnected by third cables different from the first and second cables (Figure 7, Reference 23 - third cables are the cables connecting the cache port packages; Figure 1; each cache memory is coupled to the bus and thus are interconnected to each other via the bus, Reference 4 [cable] in Figure 1).

Regarding claims 4 and 11, Ninomiya discloses that the memory units packaged in the plural memory packages store the same data (the same data stored in the memory packages is the same in that the data is received from the same sources).

Regarding claims 5 and 12, Ninomiya discloses that power is supplied from different power supplies to the plural memory packages (C 7, L 36-52).

Regarding claims 13-16 and 18-21, Ninomiya discloses a disk array controller comprising a channel interface unit to be connected with a host computer (Figure 1, Reference 1; Figure 1 shows the channel interface unit connected to a host computer via a host interface); a disk interface unit to be connected with a disk drive (Figure 1, Reference 2; Figure 1 shows the disk interface unit connected to a disk drive); a memory interface unit for storing control data for the disk drive (Figure 1, Reference 3); an interface platter in which the channel interface unit and the disk interface are mounted (C 7, L 38-41); a memory platter on which the memory unit is mounted (C 7, L 38-41; part of the unit which stores the memory unit); plural cables which couples the interface platter and the memory platter (Figure 20, References 207 –1, 207-2, 207 n-1, 207 n; 208 –1, 208-2, 208 n-1, 208 n); a selector unit, coupled with the channel interface unit, the disk interface unit and the memory unit, which selects requests from the channel interface unit and the disk interface unit (inherent, means is necessary in deciding which requests goes to what unit for proper functioning of the system); wherein a path coupling the channel interface unit to a first cable is printed in the interface platter (inherent, internal wiring connection; C 8, L 5-15, L 29-55); wherein a path coupling the disk interface unit to the second cable different from

the first cable is printed on the interface platter (inherent; internal wiring connection; C 8, L 5-15, L 29-55), and wherein a path coupling the memory unit to the third cable different from the first and second cable and is printed on the memory platter (inherent; internal wiring connection; C 8, L 5-15, L 29-55)

Regarding claim 22, 27, 30 and 38-39, Ninomiya discloses plural channel interface units each of which is coupled with a host computer (each of References 1 in Figure 1); plural disk interface units each of which is coupled with a disk drive (each of References 2 in Figure 1); plural platters on each of which the channel interface unit, the disk interface unit and memory units are mounted (each of References 56 in Figures 6A, 6B); plural cables which couple the plural platters (bus connections coupled to each Reference 56 via connectors on the backplane; Figure 20, References 207 –1, 207-2, 207 n-1, 207 n; 208 –1, 208-2, 208 n-1, 208 n); wherein a path coupling the channel interface unit to first cable is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55); wherein a path coupling the disk interface unit to a second cable, different from the first cable, is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55), and wherein a path coupling the memory unit to a third cable, different from the first and second cables, is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55).

Regarding claims 24-26 and 28-29, Ninomiya discloses a selector unit, connected with the channel interface unit, the disk interface unit and the memory unit which are mounted on one of the plural platters, which selects requests from the channel interface and the disk interface unit

(inherent, means is necessary in deciding which requests goes to what unit for proper functioning of the system).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 36-37 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya (USPN: 5,819,054).

Regarding claims 36 and 41, Ninomiya discloses a disk array controller comprising a channel interface unit to be connected with a host computer (Figure 1, Reference 1; Figure 1 shows the channel interface unit connected to a host computer via a host interface); a disk interface unit to be connected with a disk drive (Figure 1, Reference 2; Figure 1 shows the disk interface unit connected to a disk drive); a memory interface unit for storing control data for the disk drive (Figure 1, Reference 3); an interface platter in which the channel interface unit and the disk interface are mounted (C 7, L 38-41); a memory platter in which the memory unit is mounted (C 7, L 38-41; part of the unit which stores the memory unit); plural cables which couple the plural platters (bus connections coupled to each Reference 56 via connectors on the backplane; Figure 20, References 207 –1, 207-2, 207 n-1, 207 n; 208 –1, 208-2, 208 n-1, 208 n); a selector unit, coupled with the channel interface unit, the disk interface unit and the memory unit, which

selects requests from the channel interface unit and the disk interface unit (inherent, means is necessary in deciding which requests goes to what unit for proper functioning of the system); wherein a path coupling the channel interface unit to first cable is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55); wherein a path coupling the disk interface unit to a second cable, different from the first cable, is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55), and wherein a path coupling the memory unit to a third cable, different from the first and second cables, is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55). However, Ninomiya does not explicitly disclose that the interface platter is perpendicular to the memory platter. However, it is known in the art that the lay out process for elements are implemented to obtain certain goals based such as space requirements, timing parameters, delays, etc. Hence, it would have been obvious to locate the interface platter perpendicular to the memory platter in Ninomiya's system to obtain specific design goals.

Regarding claims 37 and 42, Ninomiya discloses a disk array controller comprising a channel interface unit to be connected with a host computer (Figure 1, Reference 1; Figure 1 shows the channel interface unit connected to a host computer via a host interface); a disk interface unit to be connected with a disk drive (Figure 1, Reference 2; Figure 1 shows the disk interface unit connected to a disk drive); a memory interface unit for storing control data for the disk drive (Figure 1, Reference 3); an interface platter in which the channel interface unit and the disk interface are mounted (C 7, L 38-41); a memory platter in which the memory unit is mounted (C 7, L 38-41; part of the unit which stores the memory unit); plural cables which couple the plural

platters (bus connections coupled to each Reference 56 via connectors on the backplane; Figure 20, References 207 –1, 207-2, 207 n-1, 207 n; 208 –1, 208-2, 208 n-1, 208 n); a selector unit, coupled with the channel interface unit, the disk interface unit and the memory unit, which selects requests from the channel interface unit and the disk interface unit (inherent, means is necessary in deciding which requests goes to what unit for proper functioning of the system); wherein a path coupling the channel interface unit to first cable is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55); wherein a path coupling the disk interface unit to a second cable, different from the first cable, is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55), and wherein a path coupling the memory unit to a third cable, different from the first and second cables, is printed on each of the plural platters (inherent; internal wiring connection; C 8, L 5-15, L 29-55). Ninomiya does not disclose the memory platter located between the plural interface platters. However, it is known in the art that the lay out process for elements are implemented to obtain certain goals based such as space requirements, timing parameters, delays, etc. Hence, it would have been obvious to locate the memory platter between the plural interface platters in Ninomiya's system to obtain specific design goals.

Allowable Subject Matter

6. Claims 6-7 and 31 are allowed.

Response to Arguments

7. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M (10:00 - 6:30); Tues, Thr (10:00 - 4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

July 8, 2004